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GA911 Design Kit V2.1
for Cadence Analog Artist:
User Manual

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Note: Except for this title page, this manual is identical to the document included in V2.0 of the design kit.

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1. Introduction

This document describes the Cadence Analog Artist implementation of Gennum Corporation's GA911 linear bipolar transistor array technology. This technology was earlier implemented into the Electric Design System by R.L. Wright and S.R. Penstone at Queen's University [1,2] and the Cadence Edge design system by J.A. McMahon and D.L. Luke at University of New Brunswick [3]. To the extent possible, the Cadence Analog Artist implementation parallels these implementations by offering the same functionality to the designer. In particular, this design kit builds upon the previous work performed at the University of New Brunswick. Supported design activities include schematic capture, layout editing, design rule checking, layout extraction, electrical rule checking, layout-vs-schematic checking, post-layout circuit extraction, and HSPICE/Spectre netlist generation.

This Cadence Analog Artist implementation of the GA911 technology contains updated information on design rules and electrical rules. These rules are different from previous implementations of the GA911 technology and experienced users should consult the appropriate sections of this manual for the new information. Failure to follow recommended GA911 design practices may lead to circuit failure.

This document is organized as follows:

Section 1 - Introduction

Section 2 - Installation and Setup

This section outlines the steps necessary to install the technology into the Cadence Analog Artist environment. It also describes how individual user accounts should be configured.

Section 3 - GA911 Technology Description

This section describes the technology, the array structure, and the individual devices which are available.

Section 4 - The Cadence Interface

This section forms the bulk of the Cadence interface user documentation. It begins by describing the recommended design methodology. Afterwards each design step is fully described. Its sub-sections describe schematic capture, simulation, layout editing, and physical design verification.

Section 5 - Devices

In this section each individual physical device is described in detail. In addition to presenting the device symbol and layout geometry, design guidelines, modeling, and netlist generation are also given.

Appendices

2. Installation and User Setup

This section describes the steps required to install this technology into an existing design environment already running Cadence Analog Artist, and the changes required to the designer's UNIX environment. Current users of Analog Artist, already using technologies such as Northern Telecom's CMOS4S or BiCMOS, should note the important differences in how the GA911 technology has been implemented. This technology is much more dependent upon customized SKILL routines than previous technologies. For this reason, if the interface is to function properly, these routines must be able to be located by Analog Artist after startup. Care should be taken when installing the software and setting up new designer's accounts.

The software has been developed using:

- Cadence Analog Artist version 4.4 (9504).

- Approximately 4 megabytes of disk storage for the technology files.

- A Sun workstation running SunOS 4.1.3 is assumed, but it should be possible to customize the startup script for other workstation types.

2.1 Installation (System Manager)

The following installation assumes that Cadence Analog Artist has been previously installed and that you have a copy of the GA911 Cadence Analog Artist technology files and library.

You will probably receive the software in the form of a tarfile which has been distributed via electronic mail.

1. If the README file for the GA911 Design Kit has been transferred separately, read it first.
2. Move to the directory where the technology is to be installed. Make sure you have the required permissions to be able to add files to this area. The path to the GA911 technology directory will be referred to in the remainder of this document as the \$GA911_TECH_DIR. Similarly, the directory in which Analog Artist has been installed will be referred to as the \$CDS_INSTALL_DIR.

- Example: `cd /cad/cadence/9504/tools/dfII/local/lib/ga911`

3. Extract the files from the tar archive

- `% tar xvf tarfile`

4. The following files and directories should be created:

README	README file for system administrator and users.
doc/	Documentation directory.
ga911/	Technology library containing device symbols and individual device layouts, as well as the array templates.
ga911.strmMapTable	File required for converting GDSII Stream files from/to Cadence Analog Artist database format.
layerMap	Technology file required by GDSII Stream/CIF conversion utilities.
models/	Directory containing device models for HSPICE/Spectre and PSPICE circuit simulators.
skill/	Directory containing customized SKILL routines required by the technology. Note that all GA911 technology-specific SKILL routines start with the prefix GA911.

2.2 User Setup

After the technology has been installed, users are required to modify their UNIX environments. The following setup should not present problems to users using other CMC-supported technologies with Analog Artist in addition to GA911.

1. Edit your .cshrc file located in your home directory to include the following path (if not already present) into your \$path variable (\$CDS_INSTALL_DIR must already be defined):

```
set path = ($path $CDS_INSTALL_DIR/local/bin)
```

2. Re-load your .cshrc file:

```
% source ~/.cshrc
```

3. Verify that your setup is correct by executing the following:

```
% startCds -h
```

3. GA911 Technology Description

3.1 The GA911 Technology

Gennum's GA911 technology is a tile-based linear bipolar transistor array that allows designers to create prototype IC layouts by simply connecting the array devices using a single layer of metal interconnect. The layer of interconnect is used in fabrication as the programming layer for the devices.

The arrays contain a selection of standard devices in fixed positions, usually mirrored and/or rotated copies of other similar cells. This allows the use of mirroring and rotation to achieve layout symmetry. The designer routes the interconnect metal between individual device pins to lay out the circuit. During this process the full hierarchy of the base arrays can be visually inspected for design rule errors and electrical rule errors.

The devices in the array consist of resistors (5 sizes), NPN transistors (2 sizes, 3 configurations), PNP transistors (1 size, 2 configurations), Multipurpose devices (3 sizes, 3 configurations), and bond pads (2 configurations).

Typical overall performance parameters for the technology are $f_t=300$ MHz, $V_{max}=20$ volts.

3.2 The GA911 Array Tiles

Gennum offers its GA911 array in various sizes beginning with the base array size of 50mil x 50mil up to a 250mil x 250mil array. The only array sizes which are available through CMC at the time of writing are a 100mil x 50mil (also called the 2x1 array) and a 200mil x 200mil (also called the 4x4 array). Figure 1 shows that each array is composed of just two tile types; Block Tile and Street Tile. There are sufficient components in each Block Tile to build a simple operation amplifier or gain block. The Street Tile offers a larger (nominally 18x) NPN device which is not available in the Block Tile tile.

3.3 GA911 Array Symmetry

The contents of the 2x1 array can be seen in Figure 2. It can be seen that the tiles form several lines of symmetry. This symmetry of the Block and Street Tiles allows metal interconnect routes to be easily replicated using mirroring and rotation operations.

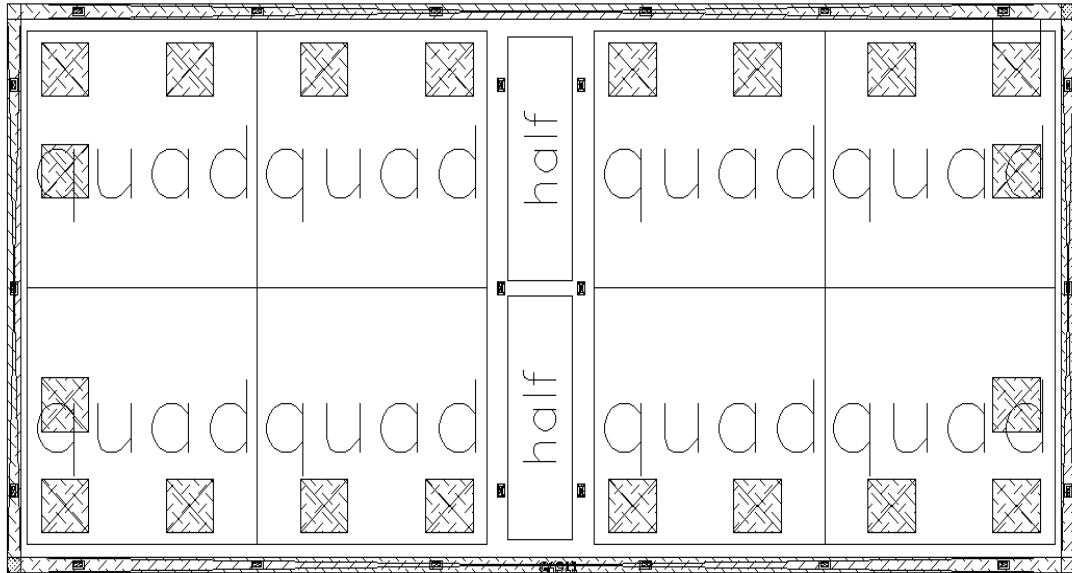


Figure 1: 2x1 Array

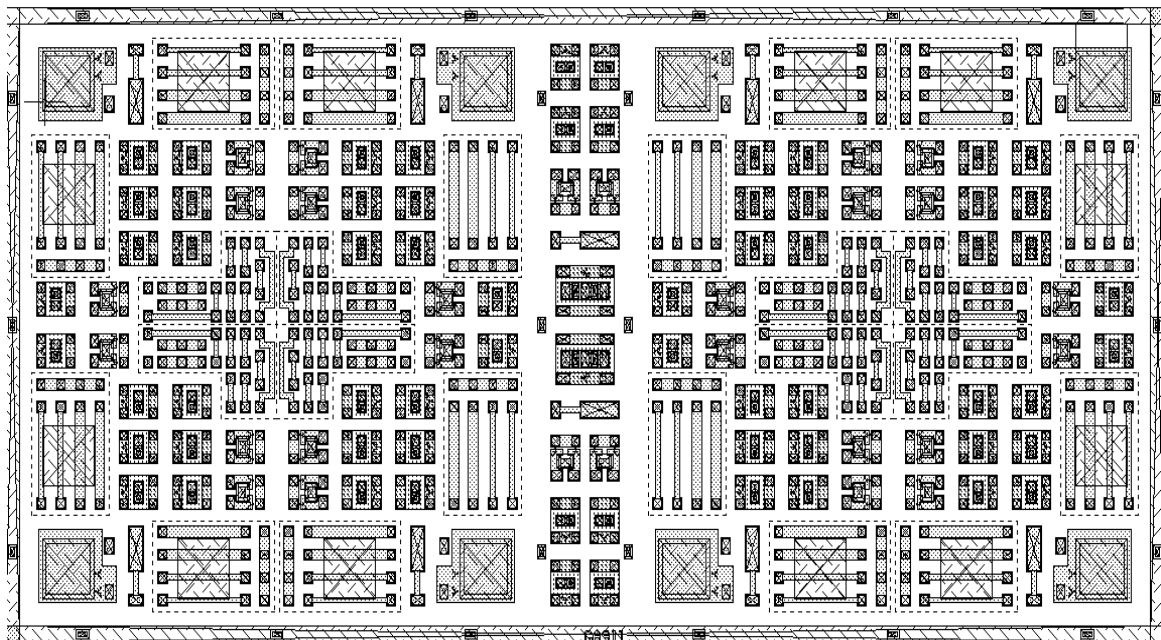


Figure 2: 2x1 Array Symmetry

3.4 GA911 Array Components

The three tables below (Tables 1-3) list the devices which are available. For the purposes of calculation, two sub-tile groupings can be used; these are the Block Tile (consisting of four Block-Quadrant tiles), and the Street Tile (consisting of two Half-Street tiles).

Table 1: Block Tile (4 Block-Quadrant Tiles) Contents

Count	Device
28	Small NPN
12	Small split-collector lateral PNP
28	P- diffused resistor (Values: 1K Ω , 5K Ω , and 10K Ω . Total:88K Ω)
8	P+ diffused resistors (Value: 200 Ω)
4	Pinch resistor (Value: 90K Ω)
4	NPN/substrate PNP/junction capacitor/low frequency bond pad
8	P- resistor cluster/high frequency bond pad

Table 2: Street Tile (2 Half-Street Tiles) Contents

Count	Device
8	Small NPN
4	Small split-collector lateral PNP
2	Large vertical NPN
2	Pinch resistor (Value: 90K Ω)

Table 3: 2x1 Array Contents

Count	Device
64	Small NPN
28	Small split-collector lateral PNP
2	Large NPN
56	P- diffused resistor (Values: 1K Ω , 5K Ω , and 10K Ω . Total: 176K Ω)
16	P+ diffused resistor (Value: 200 Ω)
10	Pinch resistors (Value: 90K Ω)
8	NPN/substrate PNP/junction capacitor/low frequency bond pad
16	P- resistor cluster/high frequency bond pad

3.5 GA911 Array Device Layouts

Figure 3 shows the layout outlines of each of the active device geometries. Note that the Small PNP Transistor is a dual collector device while the Large NPN Transistor is a dual emitter device. The 90K Ω Pinch Resistor is made using a P-type JFET device. The Multipurpose device can be configured as a NPN transistor, a PNP transistor, or a capacitor.

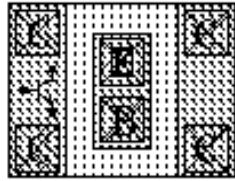


Figure 3a: *Small NPN Transistor*

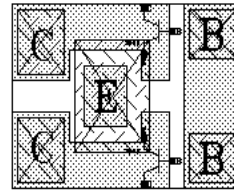


Figure 3c: *Small PNP Transistor*

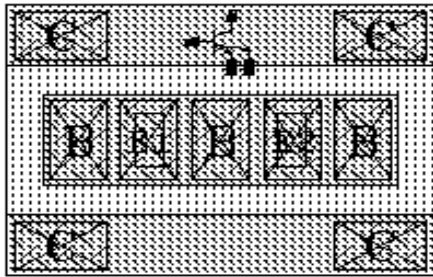


Figure 3b: *Large NPN Transistor*



Figure 3d: *90k Ω Pinch Resistor*

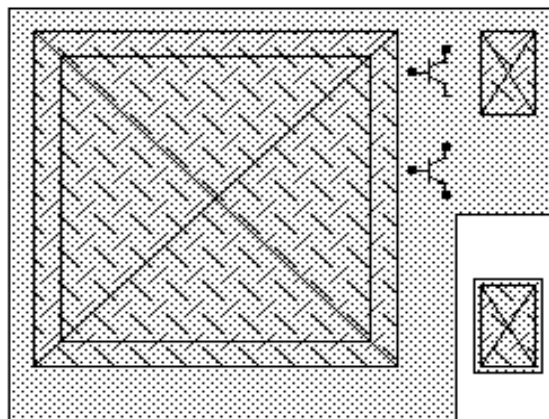


Figure 3e: *Multipurpose Device*

Figure 3: Active Device Layouts

3.6 Resistor Lands

Figure 4 shows the land areas containing the P-diffused resistors. Note that all four Block-Quadrant tiles share the common resistor land at the center of the block tile. There are four discrete resistor values available: 200Ω , $1K\Omega$, $5K\Omega$, and $10K\Omega$. Each land area containing used resistors should always be connected to the most positive chip supply voltage (vcc!) or at least be connected to circuit node which is more positive than the potential applied to any of the resistors contained in that land. Connections to a resistor land area can be made through the use of the land contacts. In the case of multiple contacts, it is only necessary to connect one of the contacts to the land bias voltage. Unused resistor lands need not be biased.

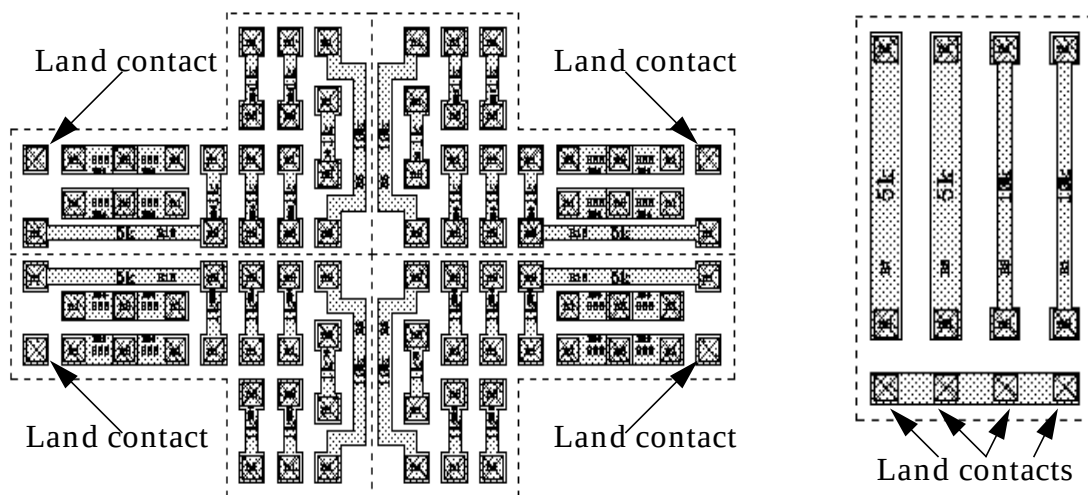


Figure 4: Resistor Lands and Land Contacts

3.7 General Layout Considerations

Circuit interconnect is performed using a single metal layer. For convenience purposes, this metal layer is actually referred to by five names; metal, vcc_metal, vee_metal, gnd_metal, and routing, depending on the purpose the layer is used for. **The actual base metal layer (metal) should NEVER be used for any purpose in your design (with the possible exception of use in a user logo generated using the CMC Gateway->Place logo menu pick in the Command Interpreter Window (CIW) menu) since it is reserved for use by Gennum.**

Many of the devices and structures used in the GA911 array also incorporate low resistance cross-unders to allow signals to cross, and these are fundamental to the layout process (see Figure 5). In some cases, the parasitic resistance and/or capacitance introduced by a cross-

under may be of concern. As a general rule always place the cross-under in the least critical signal path from the point of view of circuit operation.

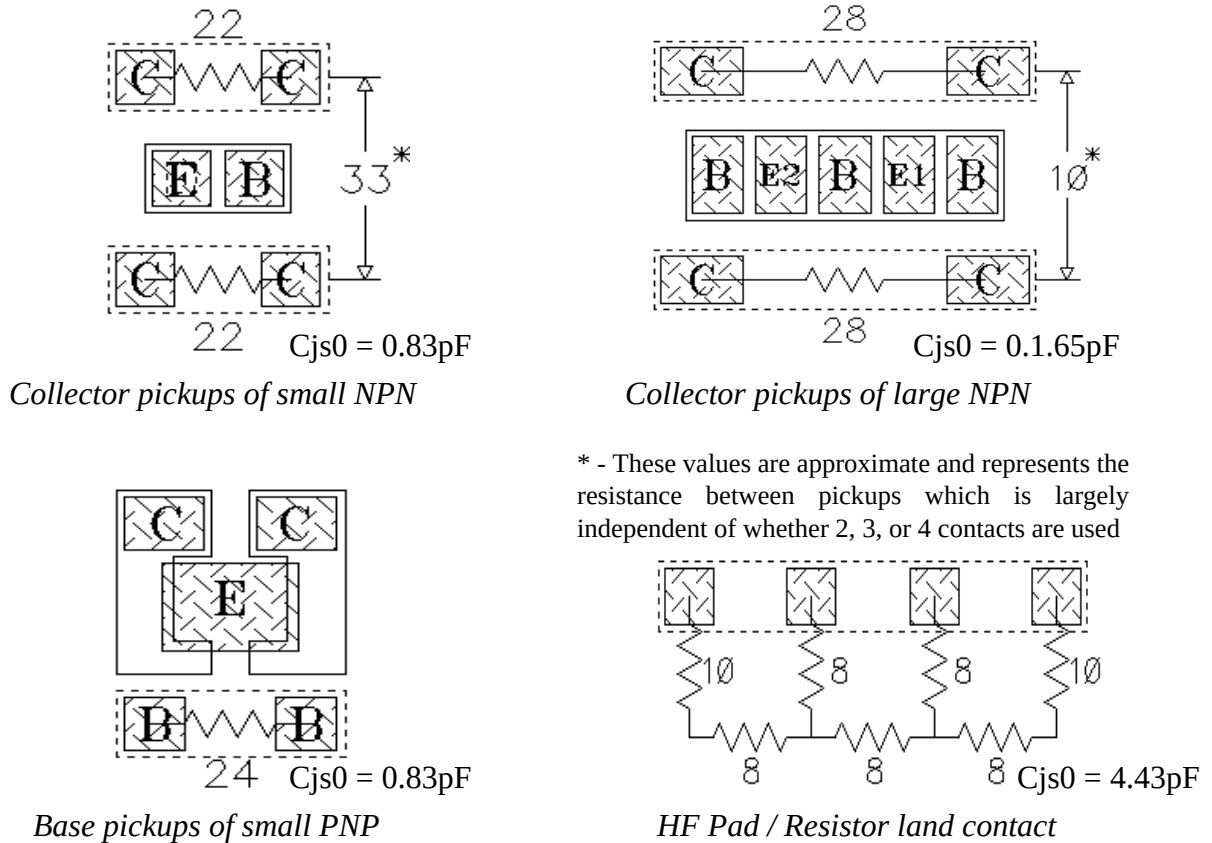


Figure 5: Cross-Unders

3.7.1 Notes on Performing Layout of Metal Interconnect

1. Non-Manhattan geometries are not recommended. Acute angles should be avoided, as should traces or polygons which overlap back onto themselves.
2. Be careful to note the orientation of the 90K Ω pinch resistor in the Street Tiles when performing mirroring operations.
3. Be aware of the 6V breakdown of the 90K Ω pinch resistor when using this device.
4. In order for LVS to compare correctly on the 90K Ω pinch resistor, care must be taken to ensure the connections are to the correct terminal.

5. The substrate should always be connected to the most negative chip supply voltage. In the GA911 technology this is vee!.
6. Resistor land areas containing used resistors should always be connected to the most positive chip supply voltage (vcc!) or at least to a circuit node which is always more positive than the potential applied to any of the resistors. It is recommended that they be connected to vcc!.

3.7.2 Layout Design Rules

1. All geometry is to be Manhattan (i.e., orthogonal).
2. No angle geometries are allowed.
3. Intersecting polygons and paths are not to be used.
4. Minimum metal track width is 6 μ m.
5. Minimum space between metal features (including notch width) is 4 μ m.
6. Metal to bond pad spacing is 26 μ m (bond pad in this context is equivalent to glass opening).

For ease of layout, the GA911 technology user should use a 10 μ m layout grid. This produces metal interconnect which is always correct by construction for the most common case of 6 μ m width metal traces (center extended), digitized onto the 10 μ m grid; the simple rule in this case is that the center lines of adjacent 6 μ m traces can occupy adjacent grid markers, while one free grid marker must be left between bond pads and adjacent 6 μ m traces.

In order to ensure a reliable design users should also refrain from long parallel runs (> 80 μ m) of metal routing. As well, large metal areas (> 80 μ m on Edge) should be avoided since they can merge with smaller, adjacent metal routing. In the latter case, if it is necessary to use the structure discussed, a separation of 8 μ m should be used.

3.7.3 Current Density Considerations

Genum recommends that the maximum current in a minimum width 6 μ m trace be kept below 5mA. For traces 12 μ m and wider, a figure of 1mA maximum per μ m is suggested.

3.7.4 Substrate Contacts

The 2x1 array and other multi-tile arrays have substrate contacts running between Block Tile and Street Tile formations (see Figure 6). In some situations where it may be convenient to use these as a connection to the negative chip supply, some caution should be exercised. The resistance from a substrate contact to the outer pickup ring is typically 70 Ω or more. Any positive current flowing into a substrate contact will raise the potential of the substrate in the

vicinity of the entering current, and this may couple any fluctuations in the current to adjacent circuit blocks and cause crosstalk or instability. In the case where the impressed voltage is greater than a few hundred millivolts, it will cause forward biasing of the epi-substrate junction which in turn will cause injection of the electrons into the substrate, usually resulting in a critical circuit malfunction.

Similar caution should be employed in the use of the substrate PNP device (where the collector current flows directly into the substrate), or an NPN device driven hard into saturation (in which case a portion of the base current flows into the substrate). In these cases it is recommended that the substrate contacts adjacent to the device should be connected directly to the outer substrate pickup ring whenever possible. Alternatively, try to use a device which is adjacent to the pickup ring.

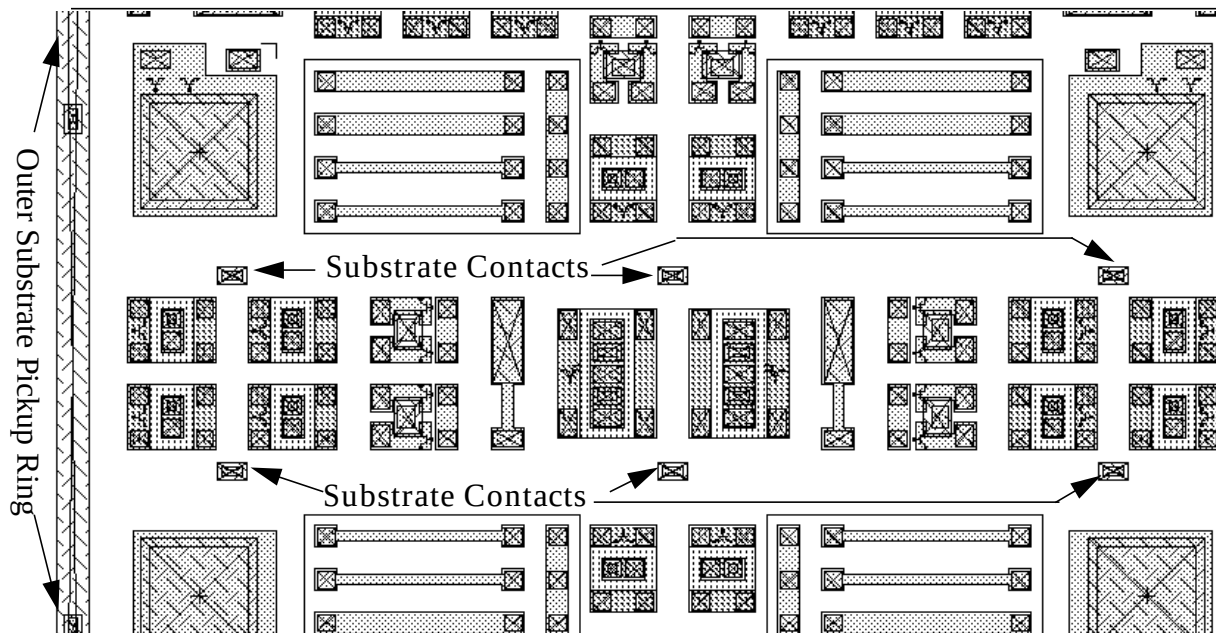


Figure 6: Substrate Contacts

3.8 Bond Pad Structures and ESD Protection Strategies

GA911 bond pad structures are designed to be multi-purpose to avoid wasted space. These are two types of bond pad structures, termed HF (for high frequency) and LF (low frequency) based on the amount of parasitic capacitance associated with the pad.

It should be noted that while a glass opening is allowed for in the pad structure no overglassing is performed for the Gennum GA911 fabrication for the CMC. Note that this lack of

overglassing is generally adequate for prototype design circuits but will affect long term yield and performance of fabricated circuits.

3.8.1 The HF Bond Pad Structure

The HF bond pad structure can either be used as a resistor cluster or as a bond pad when it occurs at the Edge of the array. **It is not recommended to use the resistors which lie beneath a used bond pad (i.e., all used HF bond pads on the Edge of the array) as they may be damaged during the pad bonding process.** In either case the land contact may be used as a cross-under. A recommended use for this cross-under is to feed the positive supply (vcc!) rail into the Block-Quadrant since this provides bias for the resistor land at the same time. The bond pad metal is electrically isolated from the underlying silicon by a layer of oxide. The resulting capacitance at the interface is approximately 0.35pF.

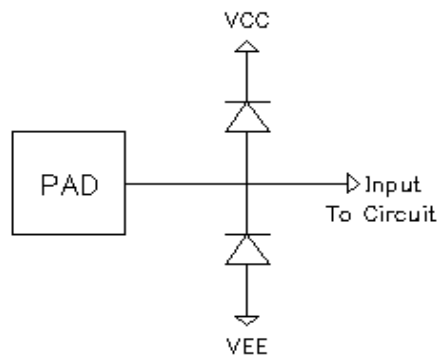
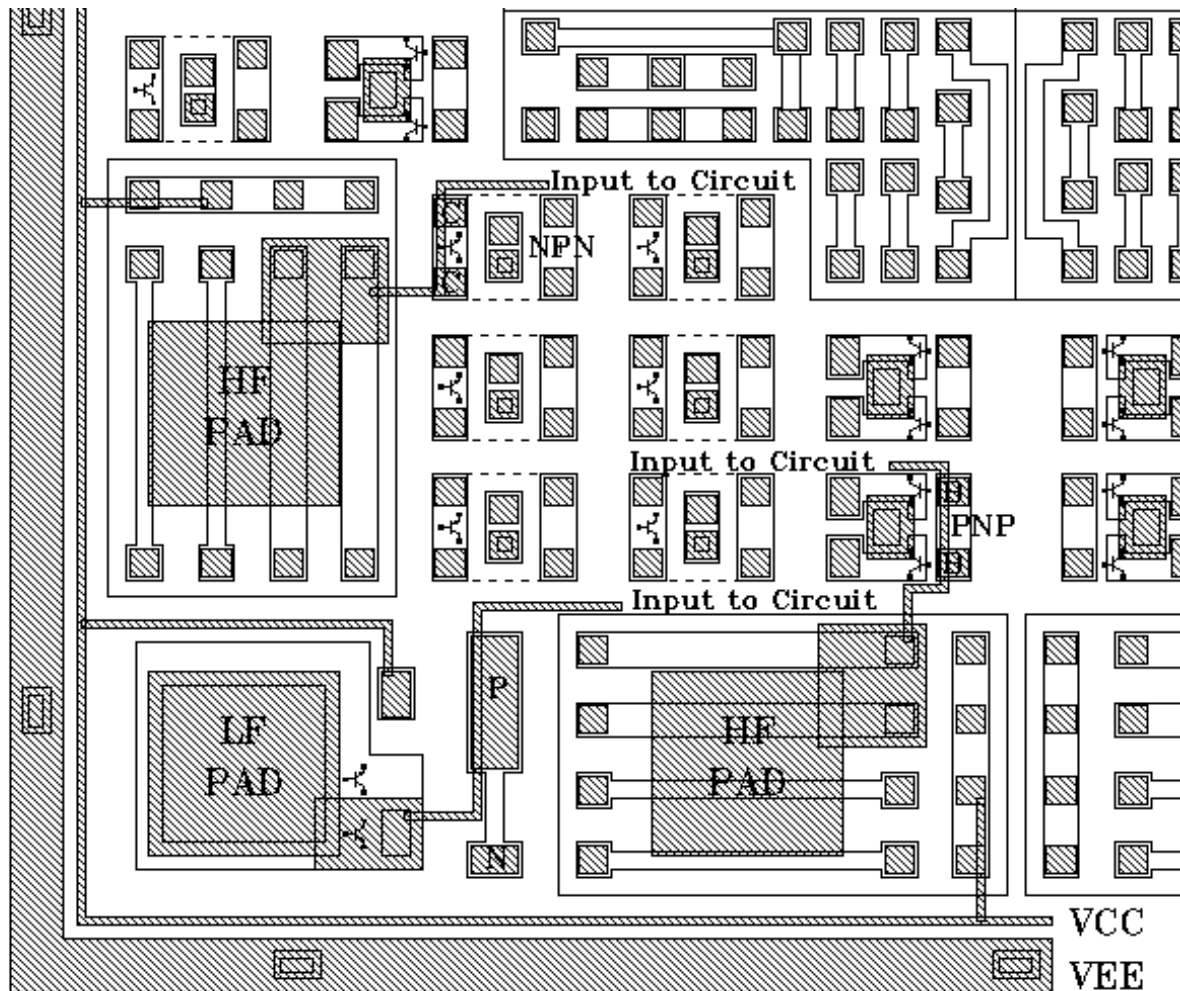
HF bond pad structures which are not at the Edge of the array have the pad metal removed to allow for more routing space. One of these areas is reserved for a CMC LOGO instance to be placed on the array before fabrication. This is done at CMC and is not to be confused with user designed logos that may be placed in unreserved areas on the array using the **CMC Gateway->Place logo** menu pick from the Command Interpreter Window (CIW) menu.

3.8.2 The LF Bond Pad Structure

The LF bond pad structure can either be used as a multi-purpose device (a large NPN transistor, a substrate PNP transistor, or a junction capacitor) or as a bond pad when it occurs at the Edge of the array. LF bond pad structures which are not at the Edge of the array retain their metal cover since it is a device contact. They cannot be bonded out. The parasitic capacitance of this pad is about 5 times higher (~1.75pF) than that of the HF bond pad due to the connections to the underlying diffusions.

3.8.3 ESD Protection

Figures 7 and 8 suggest some methods for ESD clamping of sensitive inputs. All three schemes shown are represented by the same electrical schematic; two clamping diodes from the pad to vcc! and vee! respectively to clamp voltage excursions at the pad which attempt to exceed the supply rails. The positive clamp diode is formed between the P diffusions(s) and the epitaxial layer in the tub beneath the pad, while the negative clamp diode is formed between the substrate and the epitaxial layer of any convenient (preferably adjacent) unused device (i.e., the base of a PNP, collector of a NPN, or positive end of a pinch resistor). More elaborate schemes are possible; these are left to the discretion of the designer.

**Figure 7: ESD Protection Circuit****Figure 8: ESD Protection Circuit Examples**

4. The Cadence Design Interface

This section describes how to create designs in the GA911 technology using the Cadence Analog Artist Design Framework II. It begins by giving the designer a global perspective of the recommended design methodology and then describes each step in detail.

4.1 The Cadence Startup Procedure

Before it is possible to access the GA911 technology it must be installed on your system. Please follow the instructions outlined in Section 2: Installation and Setup. Section 2 also contains instruction on how to invoke Analog Artist. This section is important because the GA911 technology requires that you do not run Analog Artist directly, instead a shell script is provided which initializes your environment and invokes the correct executables for you.

Users of the design environment should already be familiar with the basics of Cadence Analog Artist schematic and layout editing. The following Cadence Analog Artist manual references are recommended.

Design Framework, Volume I.
Design Entry
Physical Design

If simulations are to be performed, then the user should also be familiar with the Analog Artist simulation tools which are described in the following Cadence manuals:

Design Analysis, Volumes 1 and 2.
Open Simulation System, Volumes 1 and 2.
Analog Artist Users Guide

4.2 GA911 Design Flow

The GA911 design environment supports all design activities from schematic capture through to physical layout and CIF file generation for fabrication. This process is outlined in Figure 9. Note that the diagram involves three view of the design: schematic view, layout view, and extracted view.

The following assumes that you have created an appropriately named library in your directory that you will do your design(s) in. This can be accomplished using the *File->New->Library* menu pick in the Command Interpreter Window (CIW) menu.

You can then open your design. This can be accomplished using the *File->Open...* menu pick in the Command Interpreter Window (CIW) menu.

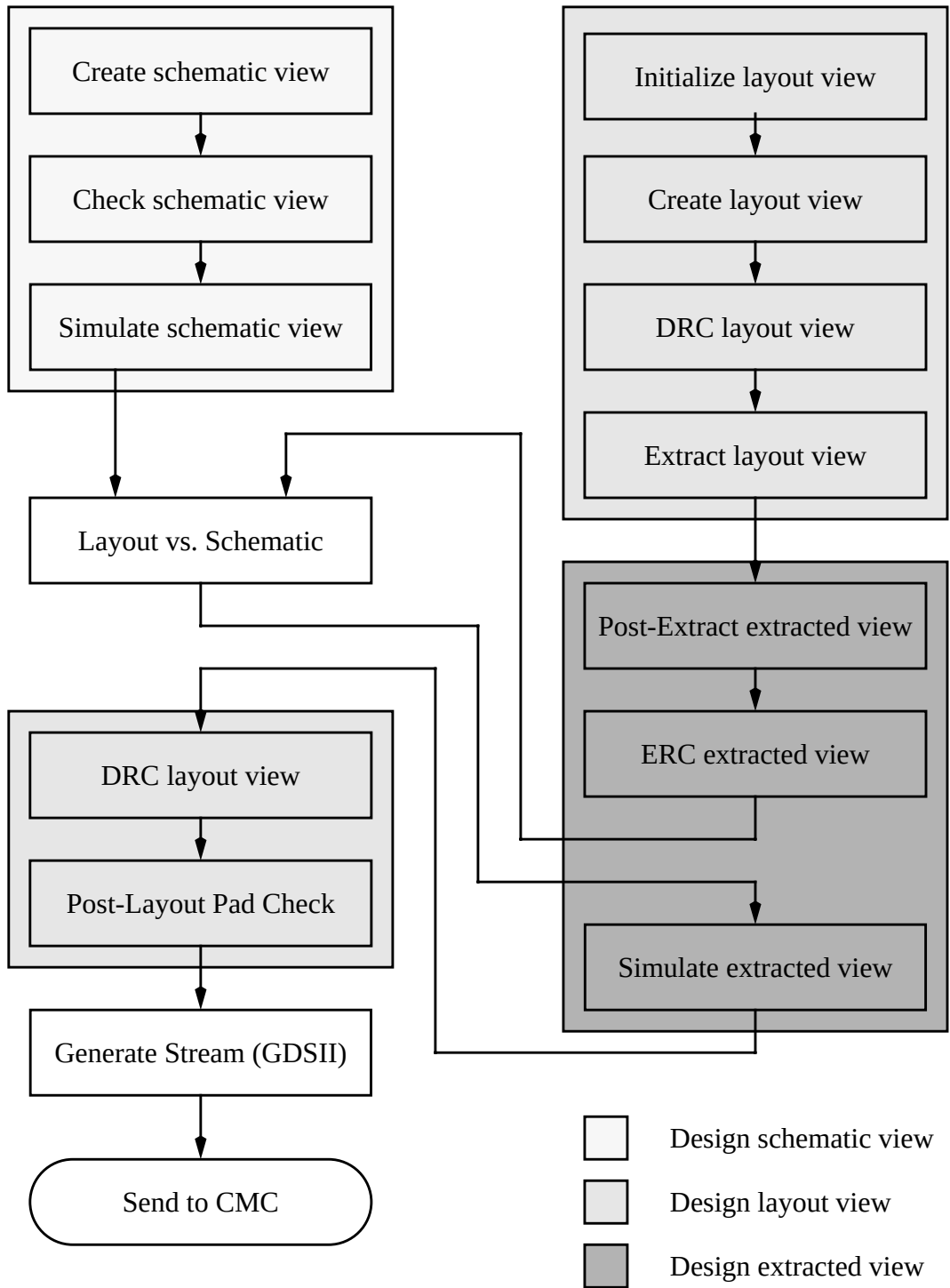


Figure 9: GA911 Design Flow

The designer usually begins by drawing the design's schematic. This is then used to generate a netlist and run an HSPICE/Spectre simulation to verify the correct circuit operation. Later the schematic can be used as guide for interconnecting the individual devices in the array. Finally, the schematic can be used to perform layout versus schematic (LVS) comparison in which connectivity of the layout is compared to the original schematic and any discrepancies are brought to the designer's attention.

For simple designs, the designer may choose not to create a schematic and proceed directly to layout phase. In this phase, the designer chooses an array template and uses metal to connect the circuit devices together. Afterwards the electrical connectivity can be extracted. At this stage it is possible to output a netlist for HSPICE/Spectre from the extracted layout data. However, it is recommended that you perform an LVS first (if a schematic is available) because it is much easier to debug a layout in this way rather than from simulation results.

The final steps of the design process require the designer to run the Design Rule Checker (DRC) on the layout data. If no problems are discovered, the design data can be converted to Stream format and sent away for fabrication. If you prefer to send the data in CIF format the Stream format can be converted to CIF format using a CMC utility program.

4.3 Creating and Editing Schematics

There are few special considerations for creating schematics in the GA911 technology. Mostly, it is just a simple matter of choosing components from the Library Browser window, placing them in the schematic, and connecting them together with wire. Some devices require that properties be added to them. For example, the generic resistor device requires that its resistance be specified. This is done by attaching a property *r* to the device. However, most active devices do not require any additional properties. Unless otherwise stated, the electrical properties of resistance and capacitance should be expressed in Ohms and Farads respectively.

4.3.1 Creating a New Schematic

To create a new schematic, you can use the ***File->New->Cellview...*** menu pick in the Command Interpreter Window (CIW).

4.3.2 Placing Components

To place a device, simply select it from the Library Manager ga911 library (symbol view) and place it in the schematic.

4.3.3 Editing Placed Components

To change properties on an instance of a device already placed in the schematic you can use the Analog Artist built-in property list editor.

4.3.4 Important Note About Analog Artist Scaling Factors

It is common practice to use the standard engineering scaling suffixes on numbers (e.g., 10K resistor) when specifying electrical properties. However, caution is required because these suffixes are all case sensitive. For example, $10M = 1 \times 10^7$ while $10m = 1 \times 10^{-2}$ (M represents Mega while m represents milli). Wrong case suffixes is a common cause of problems when running LVS. The suffix K is often the problem here because is used so often on resistors and its lowercase equivalent k is not a valid Analog Artist scaling factor. Therefore, when editing resistance values on schematics be sure to use the uppercase K.

When in doubt enter the value in exponential format (e.g., 1.0E4) and the number will be converted (if necessary) to an appropriate suffix.

4.3.5 Special Terminals

The GA911 Library menu also contains three special symbols; vcc!, vee!, and gnd!. These are used to identify global nets in the schematic. The vee! symbol is used in the array to represent the substrate - since the substrate must be connected to the lowest potential. The gnd! symbol is needed for simulation purposes (i.e., net 0 in HSPICE/Spectre).

Note that since vcc!, vee!, and gnd! are global symbols it is not necessary to wire them to the rest of the design's circuit. However, in the interest of circuit documentation, the user should always use a complete schematic that contains power supply symbols (available from the analogLib library).

In order for Layout versus Schematic (LVS) to succeed, do NOT put schematic pins on the global vcc!, vee!, and gnd! symbols in the schematic view of the design.

4.3.6 Adding Parasitic Components

Parasitic components can be added to the schematic to improve the realism of circuit simulations. You can either place a pdiode (parasitic diode) or pcapacitor (parasitic capacitor) element. For the parasitic diode you are required to specify the name of the HSPICE/Spectre model to be used during simulations (see the devices section for more details on what models are available). Similarly, for the parasitic capacitor you must add a capacitance property (c).

4.4 Simulation Support

Simulation support consists of HSPICE/Spectre netlist generation capabilities from both the schematic and extracted representations. In the Analog Artist environment the designer can use the Simulation and Waveform popup menus to create netlists, run simulations, and view waveforms. These activities are best described in the Cadence Analog Artist reference manuals Design Analysis Volumes I, II.

4.4.1 Spice Models

Three sets of Spice models have been provided: one for PSPICE (originals from Gennum, not CMC-supported) and the other two for HSPICE/Spectre (they are identical). These sets are described in Appendices 3 and 4 respectively. All models can be found in the \$GA911_TECH_DIR/models directory.

4.5 Creating and Editing Layouts

4.5.1 Initializing a New Design

Each new layout begins with the placing (see below) of an instance of one of the ga911 library layout templates into an empty layout window. The current GA911 technology only offers two template sizes; 2x1 and 4x4. However, there are six templates stored in the ga911 library: 2x1_hier, 2x1_flat, 4x4_hier40 (40 pins), 4x4_flat40, 4x4_hier44 (44 pins), and 4x4_flat44. The hier templates contains the hierarchy of Block and Street Tiles described in Section 3 while the flat templates have this level of cell hierarchy removed, revealing the individual device geometries. Otherwise the two templates are the same. The template layouts are included for user design purposes and are not to be changed in any way.

The initial placement of the chosen template is performed by the **CMC SKILL->Initialize layout** menu pick in the Layout Editor window menu. The user chooses the template (in this case hierarchical templates are used and automatically flattened to the correct levels) and executes the command. Typing f after the command has completed will allow the user to see the flattened layout.

When editing the layout be careful not to accidentally move any of the device instances inside the template. If this occurs, you can use the undo command to undo the previous edit operation or you can use the template bias layer as a guide when moving device(s) back to their original locations. If the template has been severely damaged you could also begin a new layout and copy your metal interconnect from the old design. This is particularly easy if you use the pseudo layers described below.

4.5.2 Adding Metal Interconnect to the Layout

After the layout has been initialized, you can proceed to connect devices together using the layout guidelines established in Section 2. Note that four layers of metal interconnect connect are available from the Layer Selection Window (LSW): vcc_metal, and vee_metal, gnd_metal, and routing. The last layer, routing, is the primary routing layer. The remaining three layers are optional pseudo layers and may be used by the designer to indicate power and ground connections. This is a recommended practice. However, all polygons appearing on all of the above layers are treated as the same metal layer for DRC and extraction purposes.

Drawing metal paths can be done using the **Create->Path** menu pick in the Layout Editor window menu. The resulting metal path should always be of the correct shape and width (minimum width = 6µm).

Note: Part of the array (over one or more of the internal resistor lands) has been set aside for a special CMC LOGO instance. This area is located in the upper right corner of the array (in the 2x1 array) and in the four internal corners of the array (in the 4x4 array). **Do NOT use this reserved area.**

4.5.3 Using the Bond Pads

The final step in completing the physical layout is usually connecting the external signals in your design to the bond pads which surround the array area. You should keep in mind that all pads are automatically bonded out whether they are used or not (unless they are removed from the array).

Those pads which are used should be identified by editing the pad's metal pin layer (designated by an X in the layout window). In this way you will assign terminal names to pins in your layout in the same way you are accustomed to adding terminals to schematics. In order for LVS to work, all used bond pad pins must have names corresponding to terminal names used in the schematic view of the design. These pin names will be used by the layout extractor to label the nets attached to them.

Care should be taken with respect to the pad(s) attached to the outer substrate ring. This ring must be connected to the most negative supply voltage. However, it has been labelled vee!, and any pad which is connected to this ring must therefore also be labeled vee!. Otherwise the layout extractor will report errors. Whatever pad is used for this purpose will generate a layout extractor warning message indicating that the original terminal name (i.e., PAD_12) has been overridden. Ignore this message.

4.6 Physical Design Verification

This section describes the steps that are involved in verifying the physical layout. The first part of physical design verification involves checking the topological correctness of the circuit. The steps involved include schematic checking, schematic simulation, layout extraction, electrical rule checking, layout versus schematic comparison (LVS), and layout post-extraction simulation. The schematic checking and layout post-extraction process are used to detect fundamental errors such as incompletely connected devices. Errors found at this stage should be corrected before proceeding any further. LVS comparison detects incorrectly specified schematics, incorrectly specified layout, or both. It will highlight any differences present between the schematic and its corresponding layout (using the extracted view of the layout). LVS output can be difficult to interpret and fix but ALL designs should be able to pass LVS. Of the above verification steps, the most important is the layout post-extraction simulation. Correct simulated performance usually guarantees that the chip is topologically correct. However, simulation is not always helpful when trying to determine why a circuit is not working. This is why LVS is normally run before layout post-extraction simulation.

The second part of the physical design verification process is to ensure that the layout is physically manufacturable, that is, it passes all of the design rules. This step is usually performed just before the design is extracted and prior to the design being converted into CIF for fabrication. Note that it can be performed at anytime, however. A DRC should always be performed before the layout is extracted.

4.6.1 Layout and Post-Layout Extraction

There are three steps involved in Layout and Post-Layout Extraction in this technology:

1. Layout Extraction: connectivity extraction and device recognition.
2. Post-Extraction: extraneous device removal (or pruning).
3. Post-Extraction: add parasitic components.

The first of these is performed on the layout view of the design.

The last two of these steps are performed on the extracted view of the design and may be performed sequentially and automatically using the **CMC SKILL->Extracted->Post-Extraction** menu pick in the Layout Editor window menu. They may also be performed one at a time. The advantage of the single step approach is that it gives the designer greater control over the extraction process.

It is very important that these three steps be executed in the order given above. For example, parasitics cannot be added before the extraneous devices have been removed. Otherwise isolated (floating) nodes may appear in the final extracted netlist.

4.6.1.1 Layout Extraction Options

The **Verify->Extract** menu pick in the Layout Editor window menu controls the Layout Extraction process. It allows you to perform the first step above. After the Layout Extraction is complete, the extracted view of the design will have been created.

When the **Verify->Extract** menu pick is selected, you will be asked to specify several Layout Extraction options. Below is a list of these options and the value which should be used (other options should use the default):

Extract Method?	macro cell
Join Nets With Same Name?	yes

4.6.1.2 Post-Extraction Options

The **GA911->Post-Extract** menu pick invokes a SKILL routine which controls the Post-Extraction process. It allows you to perform all three Post-Extraction steps or only the first one or two steps. After the Post-Extraction is complete, the extracted representation will replace the original extracted representation in the window where the command was called.

When selected, you will be asked to specify several Post-Extraction options. Below is a list of these options and the value which should be used (other options should use the default):

Prune unconnected devices?	Yes
Pruner to use?	Rule-Based
Add parasitics?	No
Type of parasitic?	None
Size of parasitic?	Worst-Case

1. Prune unconnected devices - Causes the device pruner to be called immediately following the connectivity extraction phase to remove extraneous (unused) devices from the extracted layout. When the pruner is activated in this way, the basic pruner will be used. For more information on device pruning, refer to the next section.
2. Pruner to use - Allows the user to specify either Basic or Rule-Based device pruning (see below).
3. Add parasitics - Causes parasitic models to be added to the extracted layout immediately following the device pruning phase. Note that parasitics will not be added unless the prune unconnected devices option has also been set to yes. For more information on adding parasitics to extracted layouts, consult the section below on adding parasitics.
4. Type of parasitics - Type of parasitics to be added to the layout. These parasitics will be added globally to all devices of the appropriate type.

5. Size of parasitics - Size of parasitics to be added to the layout. This applies to Capacitance Model parasitics added to resistors. Worst-Case and Typical are the two choices. Refer to Table 4.

4.6.1.3 The Prune Devices Option

Following the layout connectivity extraction phase you will find that all devices, whether they are part of your circuit or not, are extracted and remain part of your circuit. Before parasitics can be added or correct netlists created, the unconnected devices must be removed. This is the job of the pruner.

This option invokes the SKILL-based device pruner which removes unconnected devices from the extracted view. Below is the list of the pruning variations:

1. Basic pruner - The basic pruner function is similar to that offered by PDcompare (see section 8.5 of the Analog Artist Physical Design Verification manual). It prunes all devices having any terminals which are not connected to rest of the circuit (i.e., through other devices or input/output terminals). The pruning is iterative. If the removal of one device causes another to become unconnected, that device in turn will be pruned. This will continue until no devices remain to be pruned.
2. Rule-Based pruner - This pruner is intended to be the more user-friendly of the two pruners. In this pruner, each device type has an associated set of rules which dictate whether the device should be kept in the extracted layout, pruned outright, or reported as an error. Generally, incompletely connected devices are not removed but are reported as errors on the marker layer. The ability of this pruner to correctly recognize improperly connected devices is limited by its rule set (which is unfortunately complex due to the multipurpose nature of some of the devices). Therefore, if the designer uses a device configuration that was not foreseen by the author of the rules, possible bogus DRC errors could result. In such situations the designer should revert to the basic device pruner.

In general the Rule-Based pruner should be the one to use, especially if the Multipurpose device is being used. Always check the resulting netlist, regardless of the pruner used, to ensure correct functionality.

4.6.1.4 The Add Parasitics Option

This option calls a SKILL routine which adds parasitic models to certain types of devices. However, this function can only be used while editing the extracted view. Below is the list of parasitic extraction options:

1. None - Causes any existing parasitic models to be removed from the extracted layout.
2. Capacitor Models - Parasitic capacitors are added to all resistors and pads.
3. Diode Models - Parasitic diode models are added to all resistors and pinch resistors. Also, diodes which model E-B breakdown (diozen) are added to all NPN transistors.

Note: No parasitics should be added to the extracted layout before the device pruner has been successfully run. It can result in devices and nodes which are not connected to the rest of the circuit.

4.6.2 Design Rule Checking

Analog Artist Diva is used to perform DRC on the final layout before it is sent away to be fabricated. The design rules which are checked include:

- Metal width and separation rules
- Array alignment - devices are in the correct locations inside the array template
- Reserved areas (such as the CMC LOGO) are not used
- Unusual shapes and angles (i.e., non-Manhattan)

DRC can be run on the layout representation from the **Verify->DRC** menu pick in the Layout Editor window menu. There are two types of checking available: flat and hierarchical. Flat full is preferred in most instances because it checks all areas of the layout. Hierarchical DRC can be performed if you have edit capability on the master ga911 library (this should never be allowed for anyone other than the system administrator).

All design rule violations will be reported on the marker warning layer or marker error layer.

4.6.3 Layout versus Schematic Comparison (LVS)

Layout versus schematic (LVS) can be performed in the normal Analog Artist fashion using the functions located on the **Verify->LVS** menu pick in the Layout Editor window menu. Consult the Analog Artist Physical Design and Physical Design Verification reference manuals for more information on running LVS.

The normal option used for LVS is:

All LVS Options Off (this includes Apply rewiring).

In order to run LVS you require a schematic and an extracted representation (with unused devices pruned). Parasitics may be present in either representation but will be ignored by the comparison program provided they are given the correct name (i.e., pcapacitor and pdiode).

4.7 Utilities

4.7.1 Stream File Generation

To generate Stream Out format data use the **File->Export->Stream...** menu pick in the Command Interpreter Window (CIW) menu.

Make sure the following have been set:

Output file name (use a .sf extension).

Layer map file name (use \$GA911_Tech_DIR/ga911.strmMapTable), under **User-Defined Options**.

4.7.2 CIF File Generation

Chip designs submitted to CMC for fabrication can be in Stream GDSII format or in CIF (Caltech Intermediate Form). To simplify the steps involved in creating a CIF file from Cadence Analog Artist, a utility called strm2cif has been provided as part of the CMC Generic Environment. It is used to convert the Stream Out GDSII data (from above) into CIF format.

When creating the CIF file you will need to specify the layer mapping file (layerMap).

Never generate CIF directly from the Cadence Analog Artist database. Always use Stream format as an intermediate format before creating the CIF code.

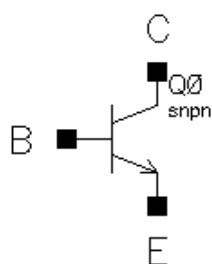
4.7.3 Plotting

The present release of the GA911 technology uses facilities existing within Cadence Analog Artist to perform plotting of schematics and layouts. Use the **Design->Plot->Submit...** menu pick in the Command Interpreter Window (CIW) menu.

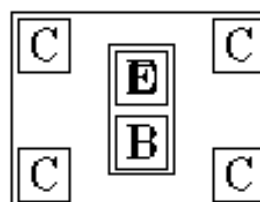
The defaults for your system should already be set up by your system administrator.

5. GA911 Devices

5.1 Small NPN Transistor (SNPN)



symbol



layout

BlockName: snpn
 ModelName: snpn_911
 HSPICE Netlist Format: Q[name] [C] [B] [E] [#vee!] snpn_911
 Spectre Netlist Format: Q[name] [C] [B] [E] [#vee!] snpn_911

Notes:

1. This device actually appears as SNPN_T in the layout.
2. The Small NPN device model includes the collector to substrate capacitance CJS and the collector to substrate diode saturation current ISS. For this reason the substrate node must be specified.
3. If the PSPICE simulator is used and a name (not a number) is used for the substrate node, it must be enclosed in square brackets. Otherwise it will be interpreted as the model name.

Parasitic models:

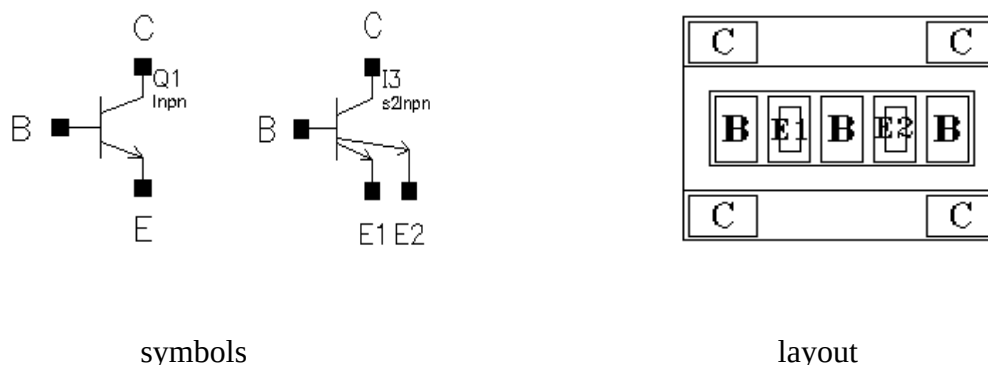
The diode parasitic diode model can be added across the emitter-base of all NPN devices for modelling the reverse emitter-base breakdown. These models will be added if you request diode models during the parasitic extraction phase. The reverse emitter-base breakdown voltage is approximately 6V.

Qzen N P N VEE snpn_911

Dzen P N diozen

The saturation current of the diode is purposely made very low so that there is negligible effect on the transistor in the normal forward operating region. The anode of the diode is connected to the base of the transistor and the cathode is connected to the emitter.

5.2 Large NPN Transistor (LNPN)



BlockNames: lnpn (single emitter), s2lnpn (dual emitter)
 ModelName: lnpn_911
 HSPICE Netlist Format: Q[name] [C] [B] [E] [#vee!] lnpn_911 (x2 if both emitters)
 Spectre Netlist Format: Q[name] [C] [B] [E] [#vee!] lnpn_911 (x2 if both emitters)

Notes:

1. The Large NPN device model includes the collector to substrate capacitance CJS and the collector to substrate diode saturation current ISS. For this reason the substrate node must be specified.
2. If the simulator PSPICE is used and a name (not a number) is used for the substrate node, it must be enclosed in square brackets. Otherwise it will be interpreted as the model name.

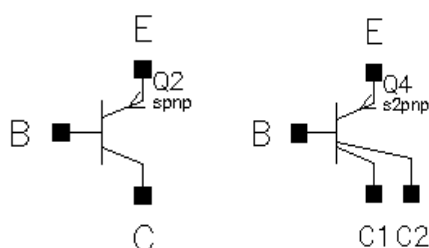
Parasitic Models:

As for the small NPN device, the diozen model may be used to model reverse emitter-base breakdown. However the diode model requires an area scaling factor of 5.5 as shown in the example below.

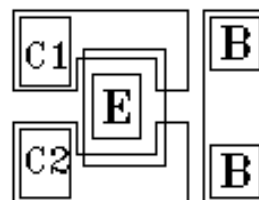
Qzen N P N VEE lnpn_911

Dzen P N diozen 5.5

5.3 Small Split-Collector Lateral PNP Transistor (SPNP)



symbols



layout

BlockName: spnp (single collector), s2np (split collector)

ModelName: spnp_911

HSPICE Netlist Format: Q[name] [C] [B] [E] [#vee!] spnp_911 0.5 (x2 if both collectors)

Spectre Netlist Format: Q[name] [C] [B] [E] [#vee!] spnp_911 0.5 (x2 if both collectors)

Notes:

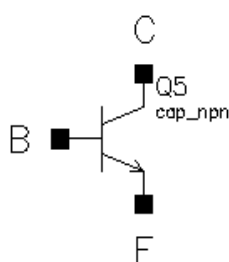
1. An unused collector MUST be tied either to a used collector or vee!. Otherwise the open collector will cause the transistor to saturate.
2. The model includes base-substrate diode capacitance, therefore the substrate terminal must be given.
3. In PSPICE this device should be modelled with the LPNP model type (see Appendix 3).

Parasitic Models:

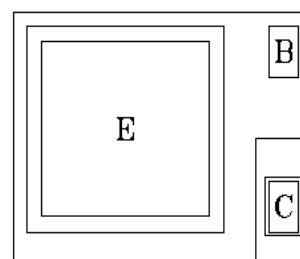
None.

5.4 Large Emitter NPN Transistor or Junction Capacitor (CAP_NPN)

This device can be created from the multipurpose device shown below and in Figure 3e. It can be used as either a very large emitter NPN transistor or a junction capacitor. The performance of this device when used as a NPN transistor limits its use to medium speed, medium to high current output buffers. As with the NPN transistor models, the substrate node is required.



symbol



layout

BlockName: cap_npn
 ModelName: cap_npn
 HSPICE Netlist Format: Q[name] [C] [B] [E] [#vee!] cap_npn
 Spectre Netlist Format: Q[name] [C] [B] [E] [#vee!] cap_npn

Notes:

1. Device configured as a 3pF capacitor (at zero reverse bias). Positive end of capacitor has approximately 3.3pF parasitic capacitance to the substrate. It has a 5V reverse breakdown voltage.

Qcap3p C+ C- C- vee CAP_NPN

2. Device configured as a 9pF capacitor (at zero reverse bias). Negative end of capacitor has approximately 3.3pF parasitic capacitance to the substrate. It has a 5V reverse breakdown voltage.

Qcap9p C- C- C+ vee CAP_NPN

3. Device configured as a 12pF capacitor (at zero reverse bias). Positive end of capacitor has approximately 3.3pF parasitic capacitance to the substrate. It has 15V reverse breakdown voltage.

Qcap12p C+ C- C+ vee CAP_NPN

Parasitic models:

The diocap parasitic diode model may be added for modelling the soft reverse breakdown of the cap_npn device, which usually occurs at a slightly lower value than the in the diozen model. Since this device also exhibits a hard breakdown, both diocap and diozen models must be used together for accurate simulation of breakdown. For example, given a 9pF capacitor:

Qcap C- C- C+ VEE cap_npn

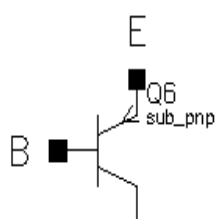
Dcap1 C- C+ diocap

Dcap2 C- C+ diozen 2.7*** Scale factor = 9pF/3.3

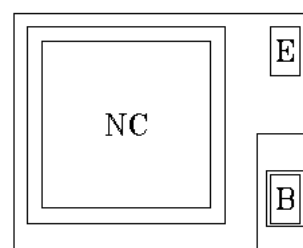
5.5 Substrate (vertical) PNP Transistor (SUB_PNP)

This device can be created from the multipurpose device shown below and in Figure 3e. The large NPN emitter diffusion must be unconnected (i.e., allowed to float). Since the collector of this device is the substrate, no explicit substrate node is required in the element specification

.



symbol



layout

BlockName: sub_pnp
 ModelName: sub_pnp
 HSPICE Netlist Format: Q[name] [#vee!] [B] [E] sub_pnp
 Spectre Netlist Format: Q[name] [#vee!] [B] [E] sub_pnp

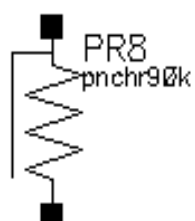
Notes:

1. LF pad (and pin) over this device must be removed before pruning.

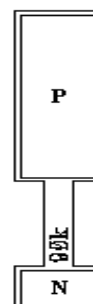
Parasitic Models:

None.

5.6 P-channel JFET 90K Pinch Resistor (PNCHR90K)



symbol



layout

BlockName: pnchr90k
 ModelName: jp90k
 HSPICE Netlist Format: J[name] [N] [P] [P] jp90k
 Spectre Netlist Format: j[name] [N] [P] [P] jp90k

Notes:

1. Terminal order is important for LVS.

Parasitic Models:

The diopin1 and diopin2 parasitic diode models can be used to model the voltage breakdown and the epi-substrate diode respectively.

Example:

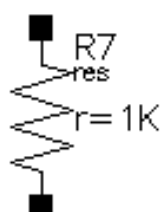
Jex N P P jp90k

Dpex1 N P diopin1

Dpex2 N P diopin2

These models are automatically added to all pinch resistors if diode models are requested during layout extraction.

5.7 Diffused Resistors



symbol

BlockNames: res200r, res1k, res5k, res5ks, res10k, res10ks
 ModelName: rp1 (except for res200r which uses rp2)
 HSPICE Netlist Format: R[name] [P] [N] rp1 <r>
 Spectre Netlist Format: R[name] [P] [N] <r>

Notes:

1. Resistor lands under used resistors must be biased (i.e., to vcc!).
2. HF pads over used resistor land areas must be removed. This is checked for at Post-Layout Pad Check time.

Parasitic Models:

The parasitic capacitance between the diffusion and resistor land can be modelled one of two ways: (1) using parasitic capacitor models or (2) with parasitic diode models.

1. Parasitic Capacitance Models - The capacitance between the resistor and its land can be represented by two capacitors (one connected to each end of the resistor) each with a value of one half of the total capacitance. The common node should be the node which is connected to the resistor land area. Different resistor sizes will have different amounts of parasitic capacitance. These models will be automatically added to all resistors during layout extraction if capacitor models have been selected. The list below gives typical worst-case capacitance values for each resistor size:

Table 4: Resistor Capacitance Values

Resistor Size	Capacitance (Worst Case)	Capacitance (Typical)
200 Ω	0.1pF	0.05pF
1K Ω	0.2pF	0.1pF
5K Ω	0.4pF	0.2pF
10K Ω	0.35pF	0.175pF

2. Parasitic Diode Models:- In place of the capacitors the dres family of parasitic diode models can be used to improve simulation accuracy. These models accurately predict the variation in capacitance with applied bias voltage. A voltage breakdown mechanism is included to catch potential problems with undervoltage resistor land bias. The forward diode characteristic is left at the default Spice settings; this is adequate for catching forward bias resistor land problems. It should be noted that under normal circumstances this situation should never be allowed to occur, as the isolation of one resistor to another in the same land will break down due to parasitic lateral PNP action (not modelled). These models will be automatically added to all resistors during layout extraction if diode models have been selected. Example: 5K resistor

R5 P N rp1 5k

Dr5p1 P [LAND] dres5k

Dr5p2 N [LAND] dres5k

References:

- [1] Wright, R.L. and Penstone, S.R., **Design Guidelines for Using the Gennum GA911 Bipolar Semicustom Array Technology with the Electric Design System**, Department of Electrical Engineering, Queen's University [January 1991].
- [2] Nairn, D.G., Penstone, S.R. and Wright, R.L., **Final Report of the Gennum Addendum to the Electric Support Contract**, Department of Electrical Engineering, Queen's University [March 1991].
- [3] McMahon, J.A. and Luke, D.L., **Gennum GA911 Technology Support for Cadence Edge**, Department of Electrical Engineering, University of New Brunswick [November 1991].
- [4] Gennum GA911 Bipolar Array Documentation, Gennum Corporation, Burlington Ontario.

Appendix 1: Known Problems and Limitations

1. When parasitic diode models are added to the extracted layout, diodes will only be added to resistors and NPN-type transistors. Parasitic diodes necessary to model the parasitic capacitance associated with the Multipurpose device (multidev), when it is used as a junction capacitor (cap_npn), are not included. These must be added manually to the netlist.
2. When using the cap_npn or sub_pnp devices in the Multipurpose device (multidev), you will have to manually remove the LF_pad and pin associated with this device context for the device pruning to work.
3. Parasitic resistances and capacitances associated with the cross-unders are not modelled. They are assumed to be zero.
4. Parasitic capacitances associated with the metal interconnect are not modelled. They are assumed to be zero.
5. In certain circumstances, the Rule-Based device pruner in the Post-Extract may not behave as desired. For example, it may generate spurious error messages or (even worse) prune a device that you want kept. Users of this pruner should be aware of its limitations. It is suggested that if this pruner causes too much difficulty that you use the Basic pruner as its behavior is much more predictable. Users should always check their HSPICE/Spectre netlist for accuracy.
6. The labelling on collectors (C), bases (B), and emitters (E) appear to be displaced when the device instance is rotated and/or mirrored. This is a bug in the way Cadence processes labels/text. It has been reported to them.
7. Other undocumented features should be reported to the CMC as soon as possible. A reward is offered!

Appendix 2: Support for Cadence Analog Artist

Support is provided for Cadence's Analog Artist design environment. The support provided is compatible with Analog Artist releases 4.4 and later.

Support consists of the following:

1. A GA911 environment compatible with the CMC Generic Environment V1.5.
2. A Cadence Analog Artist compatible library (ga911) containing:
 - all GA911 device symbols (where appropriate).
 - all GA911 device schematics (where appropriate).
 - all GA911 device layouts.
 - Component Description Format (CDF) for the following Analog Artist supported simulators; auLvs, hspiceS, and spectreS.
3. A Cadence Analog Artist compatible technology file (ga911.tf).
4. HSPICE/Spectre models for the GA911 devices.
5. A CIF layerMap file for use with strm2cif. **DO NOT USE CIF OUT OR CIF IN FOR EITHER DIRECT EXPORT OR DIRECT IMPORT OF CADENCE DATABASE DESIGN DATA. ALWAYS USE STREAM GDSII AS AN INTERMEDIATE FORMAT.** There are known bugs in directly importing or exporting CIF format design data to/from Cadence.
6. A Stream GDSII ga911.strmMapTable file for use with the generation of Stream GDSII format from Cadence database format. See point 5) above.
7. On-line documentation is available from the GA911 menu pick from within Cadence.
8. Two demo designs (in the GA911 demo library).
9. An automated method to translate Cadence Edge GA911 designs into Cadence Analog Artist. This is yet to be completed.
10. A CMC support program reachable via e-mail (support@cmc.ca) or telephone (613-530-4666).

Appendix 3: PSPICE Device Models

Genum provides one nominal and eight worst-case model parameter sets for the purpose of performing PSPICE circuit simulations. Each set has been placed in separate files in the \$GA911_TECH_DIR/models/pspice directory. The files are identified by a three-letter designation representing NPN (N) transistor beta, PNP (P) transistor beta, and diffused resistor sheet resistivity (R). Each process index can be set to either the maximum (H), minimum (L), or nominal (N) values. The eight worst-case model sets represent all possible combinations of these three parameters, which are usually the main factors influencing circuit performance. Where possible, these variables are correlated to other related device parameters to improve the realism of each of the eight worst-case scenarios. It can be assumed that the limiting values of the circuit performance obtained with these models represent the expected 3σ points on the distribution of devices in production, as long as the examined performance measures are influenced by process variations rather than by device matching considerations. For those aspects of circuit performance which are affected by device matching, this has to be dealt with separately by systematically introducing maximum offsets into matched devices, according to specifications for matching given in the representative semicustom design manual. For cases where both matching and processing affect the performance of a device, the designer should seek the global maximum and minimum by applying both techniques together.

Files:

\$GA911_TECH_DIR/models/pspice/nnn	- nominal model set
\$GA911_TECH_DIR/models/pspice/hhh	- worst-case model set
\$GA911_TECH_DIR/models/pspice/hhl	- worst-case model set
\$GA911_TECH_DIR/models/pspice/hlh	- worst-case model set
\$GA911_TECH_DIR/models/pspice/hll	- worst-case model set
\$GA911_TECH_DIR/models/pspice/lhh	- worst-case model set
\$GA911_TECH_DIR/models/pspice/lhl	- worst-case model set
\$GA911_TECH_DIR/models/pspice/llh	- worst-case model set
\$GA911_TECH_DIR/models/pspice/lll	- worst-case model set

Appendix 4: HSPICE/Spectre Device Models

Gennum does not provide HSPICE/Spectre compatible model sets with its technology. However, since HSPICE is the principal analog circuit simulation tool for CMC-supplied design kits, the PSPICE model sets have been translated into a HSPICE/Spectre compatible format. These can be found in the \$GA911_TECH_DIR/models/hspice directory and in the \$GA911_TECH_DIR/models/spectre directory.

Since the difference between the two simulator (PSPICE and HSPICE/Spectre) formats is minor, only the nominal HSPICE/Spectre model set is presented here. Changes are indicated by the comments.

Files:

\$GA911_TECH_DIR/models/hspice/nnn	- nominal model set
\$GA911_TECH_DIR/models/hspice/hhh	- worst-case model set
\$GA911_TECH_DIR/models/hspice/hhl	- worst-case model set
\$GA911_TECH_DIR/models/hspice/hlh	- worst-case model set
\$GA911_TECH_DIR/models/hspice/hll	- worst-case model set
\$GA911_TECH_DIR/models/hspice/lhh	- worst-case model set
\$GA911_TECH_DIR/models/hspice/lhl	- worst-case model set
\$GA911_TECH_DIR/models/hspice/llh	- worst-case model set
\$GA911_TECH_DIR/models/hspice/lll	- worst-case model set
\$GA911_TECH_DIR/models/spectre/nnn	- nominal model set
\$GA911_TECH_DIR/models/spectre/hhh	- worst-case model set
\$GA911_TECH_DIR/models/spectre/hhl	- worst-case model set
\$GA911_TECH_DIR/models/spectre/hlh	- worst-case model set
\$GA911_TECH_DIR/models/spectre/hll	- worst-case model set
\$GA911_TECH_DIR/models/spectre/lhh	- worst-case model set
\$GA911_TECH_DIR/models/spectre/lhl	- worst-case model set
\$GA911_TECH_DIR/models/spectre/llh	- worst-case model set
\$GA911_TECH_DIR/models/spectre/lll	- worst-case model set

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* NOMINAL HSPICE model set for GA911 semicustom array. V1.1 July 1990
* NPR = NNN (Nominal NPN Beta, Nominal PNP Beta, Nominal sheet Rho)
* HSPICE compatible - based on the nominal PSPICE model set

.MODEL SNPN_911 NPN (IS=5E-17 BF=147 VAF=80 IKF=4.3E-3 ISE=8E-18 NE=1.233
+BR=1.9 VAR=11 IKR=6E-4 ISC=5E-16 NC=1.08 RE=12 RB=1200 RBM=200 RC=25
+CJE=58E-15 VJE=0.83 MJE=0.35 CJC=133E-15 VJC=0.6 MJC=0.44 XCJC=1
+CJS=830E-15 VJS=0.6 MJS=0.4 ISS=1E-16 FC=0.85 TF=60P XTF=48 ITF=3E-2
+TR=10N EG=1.16 XTI=3 XTB=1.6)

.MODEL LNPN_911 NPN (IS=7.5E-16 BF=206 VAF=58 IKF=20E-3 ISE=8E-18 NE=1.105
+BR=4.5 VAR=11 IKR=2E-3 NC=2 RE=0.7 RB=660 RBM=35 RC=9 CJE=550E-15 VJE=0.83
+MJE=0.35 CJC=440E-15 VJC=0.6 MJC=0.44 XCJC=1 CJS=1.65E-12 VJS=0.6 MJS=0.4
+ISS=2E-16 FC=0.85 TF=70P XTF=20 ITF=0.2 TR=2N EG=1.16 XTI=3 XTB=1.6)

.MODEL CAP_NPN NPN (IS=10E-15 XTI=3 EG=1.16 VAF=31 BF=350 NE=1.45 ISE=1E-15
+IKF=0.5 XTB=1.6 BR=10 NC=2 RC=50 RB=1100 RBM=300 CJC=3.29E-12 MJC=0.44
+VJC=0.6 FC=0.85 CJE=8.8E-12 MJE=0.35 VJE=0.83 TR=10N TF=80E-12 ITF=0.3 VTF=6
+XTF=50 CJS=3.27E-12 MJS=0.4 VJS=0.6 ISS=4E-16)

* JP90K changed: BETATCE removed
.MODEL JP90K PJF (VT0=-2.65 BETA=2.3E-6 IS=1.8E-16 RS=650
+RD=3.5E3 CGD=250E-15 CGS=135E-15 M=0.38 PB=0.75)

.MODEL SPNP_911 PNP (IS=2.9E-16 XTI=3.3 EG=1.16 VAF=60 BF=49 NE=1.585
+ISE=4E-15 IKF=140E-6 XTB=1.5 BR=0.5108 VAR=6 NC=1.58 ISC=40E-15 IKR=140E-6
+RC=50 RE=20 RB=150 RBM=30 CJC=245E-15 MJC=0.44 VJC=0.6 FC=0.85 CJE=54E-15
+MJE=0.44 VJE=0.6 TF=14E-9 ITF=3E-3 VTF=4 XTF=0.8 TR=338E-9
+ISS=1E-16 CJS=830E-15 VJS=0.6 MJS=0.4)

.MODEL SUB_PNP PNP (IS=8E-15 XTI=3.3 EG=1.16 VAF=100 BF=40 NE=1.49 ISE=35E-15
+IKF=4E-3 XTB=1.5 BR=.2 VAR=20 NC=2 RE=50 RC=70 RB=200 RBM=20 CJC=3.27E-12
+MJC=0.4 VJC=0.6 FC=0.85 CJE=3.29E-12 MJE=0.44 VJE=0.6 TR=633E-9 TF=10E-9
+ITF=30E-3 VTF=50 XTF=1.2)

* RP1 changed: TC1->TC1R, TC2->TC2R
.MODEL RP1 R SCALE=1.0 TC1R=1.12E-3 TC2R=2.81E-6

* RP2 changed: TC1->TC1R
.MODEL RP2 R SCALE=1.0 TC1R=1.06E-3

.MODEL DIOPIN1 D (IS=1E-25 RS=3.5E3 BV=6.2 IBV=1E-5)

.MODEL DIOPIN2 D (IS=2E-16 RS=450 CJO=892E-15 M=0.4 VJ=0.6)

.MODEL DIOCAP D (IS=1E-25 RS=310 BV=5.65 IBV=1E-5)

.MODEL DIOZEN D (IS=1E-25 RS=220 BV=5.95 IBV=1E-5)

.MODEL DRES200R D (CJO=5E-14, M=0.44, VJ=0.6, BV=18, IBV=1E-5, RS=150)

.MODEL DRES1K D (CJO=1E-13, M=0.44, VJ=0.6, BV=18, IBV=1E-5, RS=150)

.MODEL DRES5K D (CJO=2E-13, M=0.44, VJ=0.6, BV=18, IBV=1E-5, RS=150)

.MODEL DRES10K D (CJO=18E-14, M=0.44, VJ=0.6, BV=18, IBV=1E-5, RS=150)

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Appendix 5: Translation of Cadence Edge Files

Contact CMC for assistance: support@cmc.ca